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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/580,160	05/30/2000	Vladimir Kostadinov	FOM-118.01	1358
25181	7590	09/26/2005	EXAMINER	
FOLEY HOAG, LLP PATENT GROUP, WORLD TRADE CENTER WEST 155 SEAPORT BLVD BOSTON, MA 02110			MIRZA, ADNAN M	
			ART UNIT	PAPER NUMBER
			2145	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/580,160

Applicant(s)

KOSTADINOV, VLADIMIR

Examiner

Adnan M. Mirza

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevenson et al (6,738,388) and Wadsworth et al (U.S. 6,067,407).

As per claims 1, 11, 15 Stevenson disclosed a method for modifying memory on at least one control device, from a remote host device (col. 8, lines 18-27), without interrupting the operation of the at least one control device, wherein the at least one control device and the host device are coupled through a Field bus communications network, the method comprising: transferring data from the host device to the at least one control device during unscheduled communications periods; storing the transferred data to respective inactive memory area (col. 21, lines 51-67 & col. 22, lines 1-29);

However Stevenson did not go in details redirecting at least one control instrument microprocessor, during an idle period of the at least one control device microprocessor.

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In the same field of endeavor Soltis disclosed the SCSI Mode and Mode select commands allow access to and modification of a SCSI-defined Device Locks mode page on the storage device (col. 25, lines 21-23). According to one aspect of the invention, the Mode sense and Mode Select commands are used for configuring the device locks on a storage device typically includes several SCSI-defined pages of configuration data (col. 25, lines 27-31).

However Stevenson-Soltis did not disclose in detail to execute the stored data in the inactive memory area to modify the processing on the at least one control device.

In the same field of endeavor Wadsworth disclosed the capability of the MLID to retrieve and store data at indicated locations in the memory of the network interface controller (col. 11, lines 26-28). Enter data is used to modify the data values, to modify process steps, to set break points for subsequent initiation of execution of the interactive debugger (col. 13, lines 26-29).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have incorporated the capability of the MLID to retrieve and store data at indicated locations in the memory of the network interface controller (col. 11, lines 26-28). Enter data is used to modify the data values, to modify process steps, to set break points for subsequent initiation of execution of the interactive debugger as disclosed by Wadsworth in the method of Steveneson-Soltis to increase the manageability of the available capacity of the disk drives and memory devices while in service in various data processing systems.

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3. As per claim 2 Stevenson-Soltis-Wadsworth-Wadsworth comprising verifying the stored data in the respective inactive memory areas (Soltis, col. 22, lines 54-64).
4. As per claims 3,12 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein redirecting at least one control device microprocessor comprises providing the at least one control device microprocessor with entry points to the stored data (Soltis, col. 20, lines 7-23).
5. As per claim 4 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein transferring data further comprises transmitting entry points (Soltis, col. 20, lines 7-23).
6. As per claim 5 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein transferring data further comprises transmitting executable instructions (Stevenson, col. 27, lines 52-65).
7. As per claim 6 Stevenson-Soltis-Wadsworth disclosed wherein transferring data further comprises synchronizing data transmissions between the host device and the control devices to avoid interference with scheduled communications (Stevenson, col. 15, lines 34-43).
8. As per claims 7,18 Stevenson-Soltis-Wadsworth disclosed selecting the respective at least one active memory area; and, inactivating the selected active memory area such that the microprocessor does not execute data in the selected active memory area (Soltis, col. 22, lines 47-50).

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9. As per claims 8,16 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein redirecting the microprocessor further comprises issuing an upgrade request from the host device to the at least one control device (Soltis, col. 21, lines 25-28).

10. As per claims 9,17 Stevenson-Soltis-Wadsworth disclosed wherein issuing an upgrade request comprises coordinating at least one upgrade command from the host device to the at least one control device (Soltis, col. 21, lines 25-35).

11. As per claim 10 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein redirecting the microprocessor further comprises: monitoring at least one parameter; and, communicating a command to redirect the at least one control device microprocessor when the parameter attains a specified value (Soltis, col. 17, lines 55-62).

12. As per claim 13 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein the at least one control device microprocessor comprises a memory verification module (Stevenson, col. 3, lines 50-67).

13. As per claim 14 Stevenson-Soltis-Wadsworth-Wadsworth disclosed wherein: the at least one active memory area comprises flash memory; and, the at least one inactive memory area comprises flash memory (Stevenson, col. 20, lines 30-50).

Response to Arguments

Applicant's arguments filed 10/04/2004 have been fully considered but they are not persuasive.

Response to applicant's arguments is as follows:

14. Applicant argued that prior art did not disclose two or more microprocessor controlled devices and also writing and/or storing to an inactive memory area during a microprocessor idle period.

As to applicant's argument Soltis disclosed SCSI Mode and Mode select commands allow access to and modification of a SCSI-defined Device Locks mode page on the storage device (col. 25, lines 21-23). One ordinary skill in the art at the time of the invention can interrupt the SCSI device as control device with microprocessor.

15. Applicant argued that prior art did not show motivation to combine references.

As to applicants argument Soltis disclosed in the method of Stevenson server based architecture that help maintaining for controlling access to shared storage devices and make it more fault tolerant. The above statement will serve as an obvious statement to combine the two prior arts.

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16. Applicant argued that prior art did not disclose “transferring data from a remote host device to at least one control device during unscheduled communications periods and without interrupting the operation of the control device”.

As to applicant’s arguments Stevenson disclosed the “shadow function block communicates with the external function blocks using the communication protocol associated with the external function blocks which may be, and typically is, different than the controller configuration protocol used by the controller to implement communications between the function blocks internal to the controller” (col. 17, lines 66-67 & col. 18, lines 1-5). One ordinary skill in the art at the time of the invention interrupted the external blocks as remote device. Any device external to the network represented as remote device. Stevenson also disclosed “ Instead the communications between the actual function block and the shadow block occur automatically without the intervention by the process control routine (col. 18, lines 63-66).

17. Applicant argued that prior art did not disclose “redirecting at least one control device microprocessor, during an idle period of the control device microprocessor, to execute the stored data in the inactive memory area”.

As to applicants arguments Soltis disclosed “the SCSI Mode and Mode select commands allow access to and modification of a SCSI-defined Device Locks mode page on the storage device. According to one aspect of the invention, the Mode sense and Mode Select commands are used for configuring the device locks on a storage device typically includes several SCSI-defined

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pages of configuration data". One ordinary skill in the art at the time of the invention interrupted the inactive memory as any storage device that has the storing capability.

Conclusion

18. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Adnan Mirza whose telephone number is (571)-272-3885.

19. The examiner can normally be reached on Monday to Friday during normal business hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Valencia Martin Wallace can be reached on (571)-272-6159. The fax for this group is (703)-746-7239.

20. The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703)-746-7239 (For Status Inquiries, Informal or Draft Communications, please label "PROPOSED" or "DRAFT");

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(703)-746-7239 (For Official Communications Intended for entry, please mark "EXPEDITED PROCEDURE"),

(703)-746-7238 (For After Final Communications).

21. Any Inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

Any response to a final action should be mailed to:

BOX AF

Commissioner of Patents and Trademarks Washington, D.C. 20231

Or faxed to:

Hand-delivered responses should be brought to 4th Floor Receptionist, Crystal Park II,
2021 Crystal Drive, Arlington, VA 22202.

AM

Adnan Mirza

Examiner

[Signature]
RUPAL DHARIA
PATENT EXAMINER